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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,900	12/24/2003	Joon-Kyu Park	8733.891.00-US	9191
30827 7590 02/01/2007 MCKENNA LONG & ALDRIDGE LLP 1900 K STREET, NW WASHINGTON, DC 20006			EXAMINER DINH, DUC Q	
			ART UNIT	PAPER NUMBER
			2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/743,900	PARK, JOON-KYU	
	<b>Examiner</b>	<b>Art Unit</b>	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>08/30/06</u> . | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This Office Action is responsive to the Applicant's Amendment filed on October 25, 2006. Claims 1-16 are pending in the Application, claims 1, 6 and 13 are currently amended.

#### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyazawa (U.S. Patent No. 6,858,991).

In reference to claim 1, Miyazawa discloses an organic electroluminescent device (in Fig. 7) comprising:

- a substrate (120);
- a gate line on the substrate (Y1);
- a data line (X1) crossing the gate line to define a pixel region (20);
- a power line (L1, L2) substantially parallel to and spaced apart from the gate line (Y1);
- a first switching thin film transistor ("Trs" see the detailed structure of pixel 200 in Fig. 8) connected to the gate line (Yn) and the data line (Xm);
- a first driving thin film transistor (Tdr) connected to the first switching thin film transistor (Trs) and the power line (L2);

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a storage capacitor (C1) connected to the first driving thin film transistor (Trd) and the power line (L2);

an organic electroluminescent diode (210) connected to a drain terminal of the first driving thin film transistor (Trd);

a gate driver (130 in Fig. 7) connected to the gate line (Yn);

a data driver (140 in Fig. 7) connected to the data line (Xm); and

a power control driver (150 in Fig. 7) supplying a power voltage to a source terminal of the first driving transistor (Trd) through the power line (L2), the power voltage having a first value during an emitting time section (Tel in Fig. 9) of a single frame (Tc) and a second value during a rest time section (Trp) of the single frame (Tc) [the electrical current through the path of the voltage supply line VL supplying from the power control circuit 150 supplying a voltage VC1 corresponding to the data current Idata which flows ... and this voltage is applied to the gate of the driving transistor... as a result, the electrical current Ids flows through the driving transistor Trd, and the OLED element begins to emits light in the light emitting period Tel; and power control driver 150 provide a second value during the writing period (not emitting light period) as shown see Fig. 8 and 9, col. 16, lines 49 – col. 17, line 6).

In reference to claim 2, Miyazawa discloses in Fig. 7, the gate driver (130) is disposed at a first side of the substrate (left side of the substrate panel 120), wherein the data driver (140) is disposed at a second side adjacent to the first side (140 is disposed in the upper side of the substrate 120 adjacent to the first side), wherein the power control driver (150) is disposed at a third side opposite to the first side (power control driver circuit is disposed at a third side as claimed; see Fig. 10).

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In reference to claim 3, Miyazawa discloses the organic electroluminescent device emits light during the emitting time (Tel) section and does not emit light during the rest time section (Trp; see Fig. 9).

In reference to claim 4, Miyazawa discloses in Fig. 8 that driving thin film transistor (Trd) has a driving gate electrode (Vg), a driving source (Vs) electrode and a driving drain electrode, wherein the storage capacitor (C1) is connected to the driving gate electrode (Vg).

In reference to claim 5, Miyazawa disclose second switching thin film transistor (Q) connected to the first switching thin film transistor (Trs) and a second driving thin film transistor (Trc) connected to the first driving thin film transistor (Trd) and the second switching thin film transistor (Q) [see Fig. 8].

In reference to claim 6, Miyazawa discloses an organic electroluminescent device (in Fig. 7), comprising:

a display panel (120) including a gate line (Y 1), a switching thin film transistor (Trs) connected to the gate line (Y1) and data line (X1), a driving thin film transistor (Trd) and an organic electroluminescent diode (20), wherein gate (at Vg), source (at Vs) and drain (at Ids) of the driving transistor (Trd) are connected to the switching transistor (Trs) a power line (L2) and the organic electroluminescent diode, respectively (See Fig. 7)

a gate driver (130) supplying a gate signal to the gate line (Y1);

a data driver (140) supplying a data signal to the data line;

a power control driver (150) supplying a power voltage to the power line (L1), the power voltage having a first value during an emitting time (Tel) section of a single frame (Tc) and a

second value during a rest time section (Trp) of the single frame (see rejection of claim 1 and Fig. 9)

In reference to claim 7, Miyazawa discloses the organic electroluminescent device emits light during the emitting time (Tel) section and does not emit light during the rest time section (Trp) (see Fig 9).

In reference to claim 8, Miyazawa discloses the device comprising a power block (as can be seen in Fig. 8 the voltage Vdd is inherently supplied from a power source block) supplying an ON voltage to the power control driver (150), wherein the ON voltage has one value in the single frame (the ON voltage Vdd to the power control circuit 150 to emit light in the light emitting period Tel; see Fig. 9 and col. 15, lines 30-40).

In reference to claim 9, Miyazawa discloses the power control driver (150) processes the ON voltage to be the power voltage (see Fig. 9, col. 15, lines 30-40).

In reference to claim 10, Miyazawa discloses the power line (L1 and L2) is substantially parallel to and spaced apart from the gate line (Y1 see Fig. 10).

In reference to claim 11, Miyazawa discloses the display panel further includes a switching thin film transistor (Trs) connected to the gate line (Yn) and the data line (Xm), a driving thin film transistor (Trd) connected to the switching thin film transistor (Trs) and the power line (L2) and a storage capacitor (C1) connected to the driving thin film transistor (Trd) and the power line (L2) [see Fig. 8].

In reference to claim 12, Miyazawa discloses the gate signal and the data signal are applied to the switching thin film transistor (Trs), wherein the power voltage is applied to the organic electroluminescent diode (210) [see Fig. 7 and 8; col. 14, lines 48-67]

In reference to claim 13, Miyazawa discloses driving method of an organic electroluminescent device (120) having a driving circuit (130-140) and a display panel (120), comprising:

applying a gate signal (scanning signal) to a switching thin film transistor (Trs) of the display panel (120);

applying a data signal (Idata) to a driving thin film transistor (Trd) of the display panel (120) through the switching thin film transistor (Trs);

applying a first value of a power voltage through a source terminal (at  $V_s$  in Fig. 8) of the driving transistor (Trd) to an organic electroluminescent diode (210) that is connected to a drain terminal (at  $I_{ds}$ ; Fig. 8) of the driving transistor (Trd) during an emitting time ( $T_{el}$ ) section of a single frame ( $T_c$ );

applying a second value of the power voltage through the source terminal (at  $V_s$  of Fig. 8) through the source terminal of the driving transistor (Trs) to the organic electroluminescent diode (210) during a rest time section ( $T_{rp}$ ) of the single frame gate ( $T_c$ ) [see the rejection as applied to claim 1].

In reference to claim 14, Miyazawa disclose the driving circuit includes a gate driver (130), a data driver (140) and a power control driver (150) [see Fig. 10].

In reference to claim 15, Miyazawa discloses the gate signal is supplied from the gate driver (130), wherein the data signal is supplied from the data driver (140), wherein the power voltage is supplied from the power control driver (150) [see Fig. 7, col. 14 lines 45-60].

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In reference to claim 16, Miyazawa discloses the gate signal turns ON/OFF the switching thin film transistor, wherein the data signal turns ON/OFF the driving thin film transistor (see Fig. 7, col. 14 lines 47-53).

*Response to Arguments*

4. Applicant's arguments filed October 25, 2006 have been fully considered but they are not persuasive. Applicant's argument, see pages 5-6 of the Remarks, "none of the cited references singly or in combination, teaches or suggests features of claimed limitations in independent claims 1, 6 and 13. However, upon reconsideration, Miyazawa (U.S Patent No. 6,858,991) as discussed above teaches the claimed limitations in Fig. 8 as elaborated in the rejections applied to claims 1, 6 and 13. Therefore, the rejection for the application is maintained.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.



*Conclusion*

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DUC Q DINH/  
Examiner  
Art Unit 2629  
DQD

January 24, 2007



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